

"SELF-ALIGNED PROCESS USING INDIUM GALLIUM ARSENIDE ETCHING TO FORM REENTRY FEATURE IN HETEROJUNCTION BIPOLAR TRANSISTOR"

Scott A. McHugo et al.

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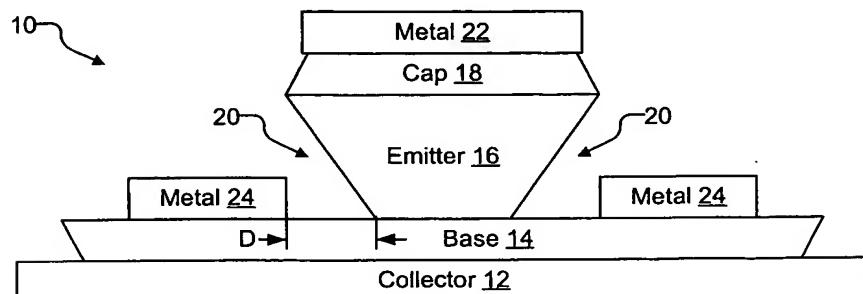


Fig. 1
(Prior Art)

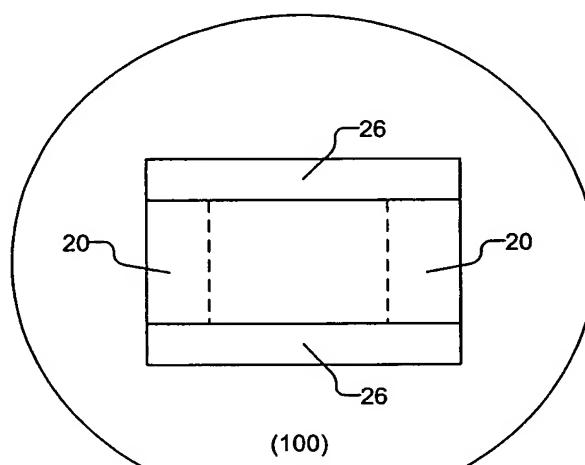


Fig. 2A
(Prior Art)

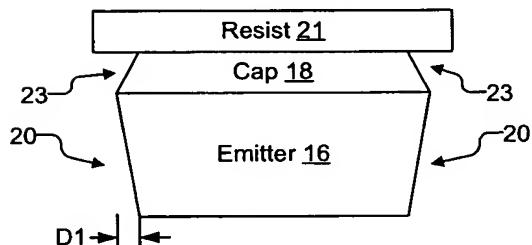


Fig. 2B
(Prior Art)

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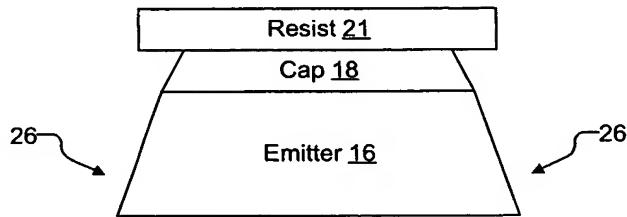


Fig. 2C
(Prior Art)

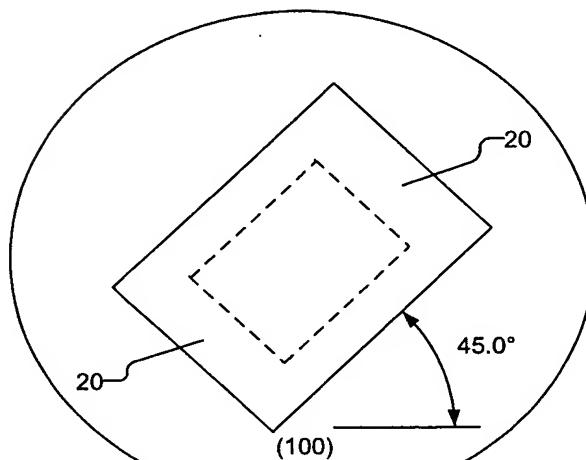


Fig. 3A
(Prior Art)

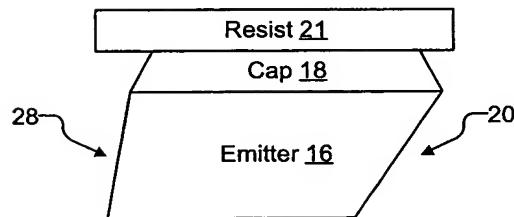


Fig. 3B
(Prior Art)

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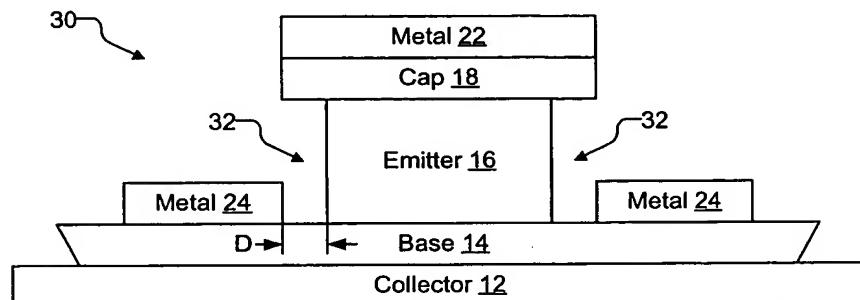


Fig. 4
(Prior Art)

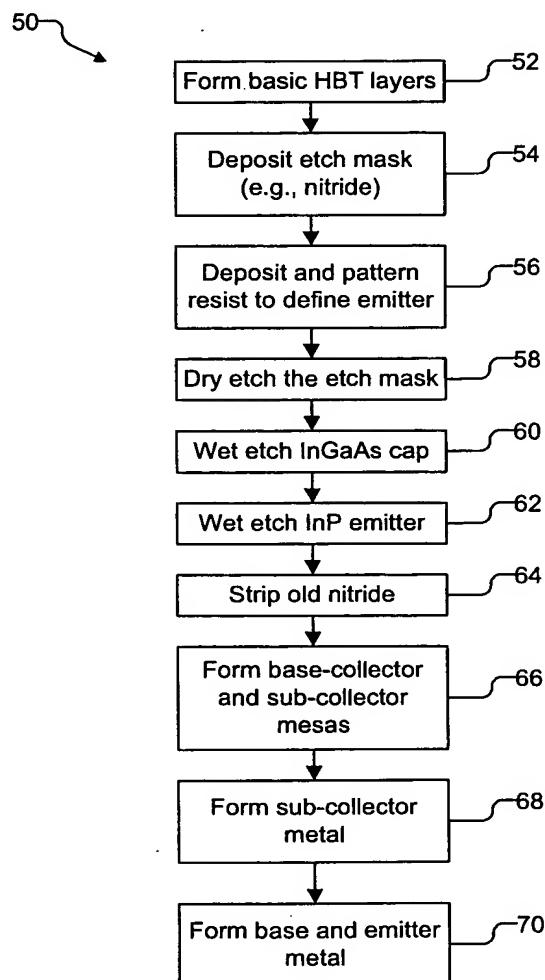


Fig. 5

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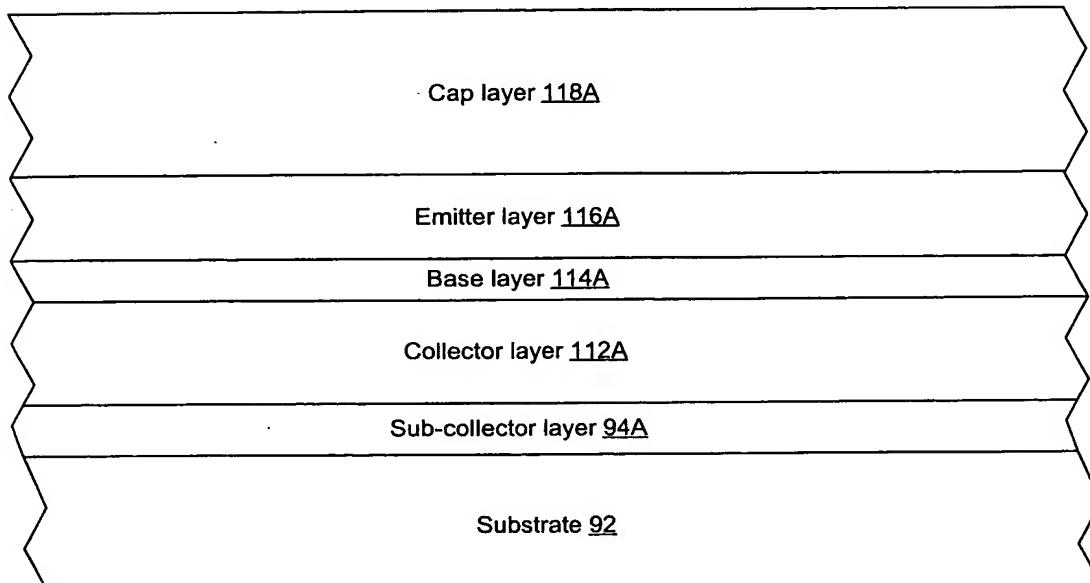


Fig. 6A

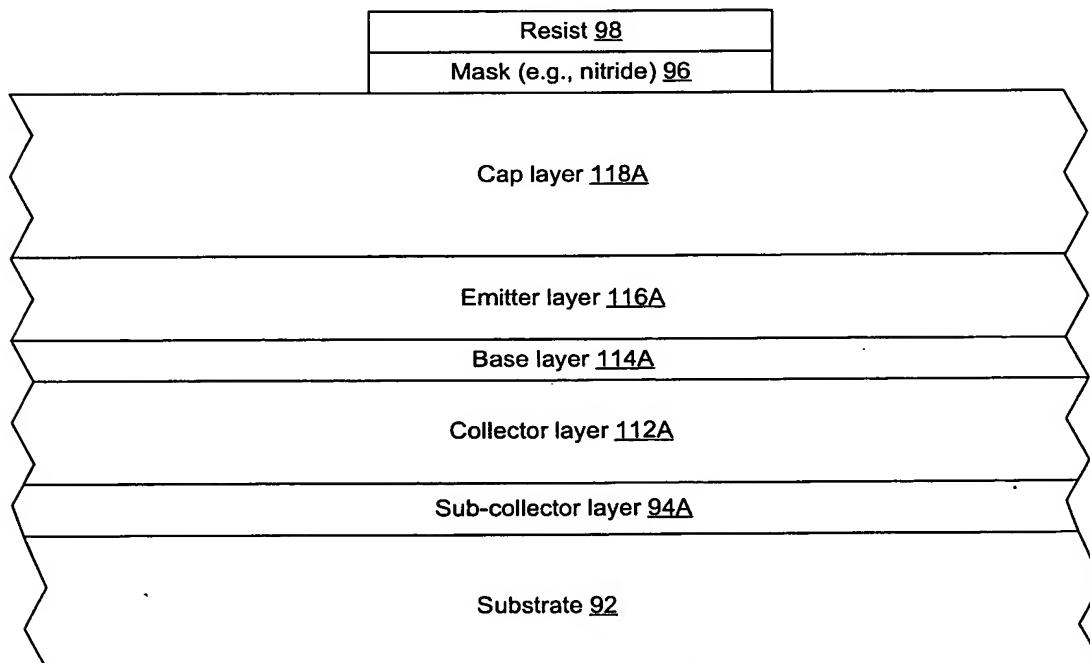


Fig. 6B

"SELF-ALIGNED PROCESS USING INDIUM GALLIUM ARSENIDE ETCHING TO FORM REENTRY FEATURE IN HETEROJUNCTION BIPOLAR TRANSISTOR"

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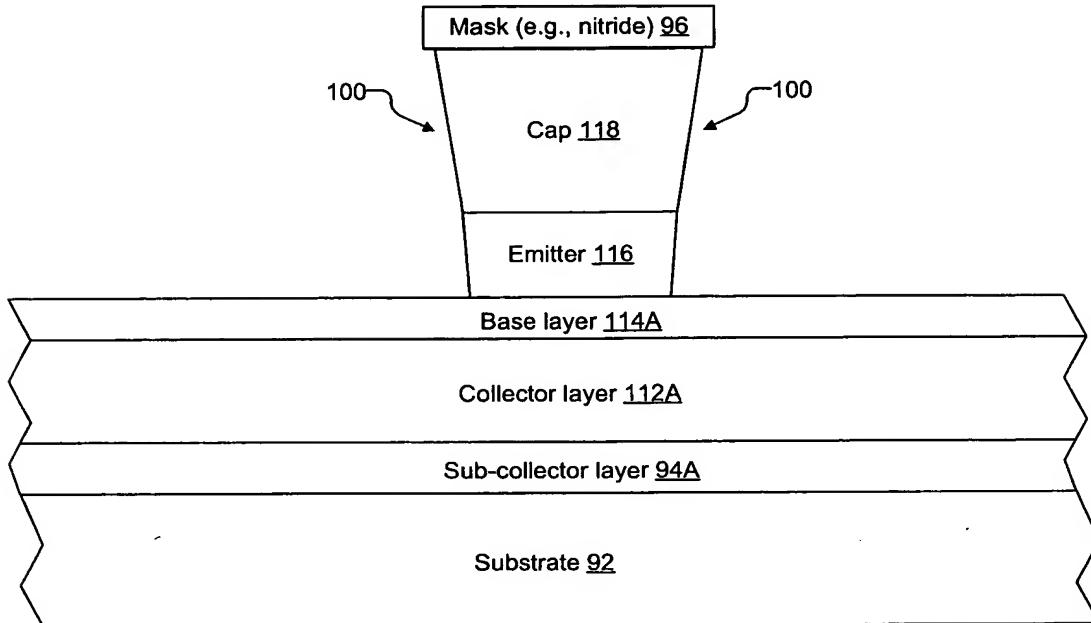


Fig. 6C

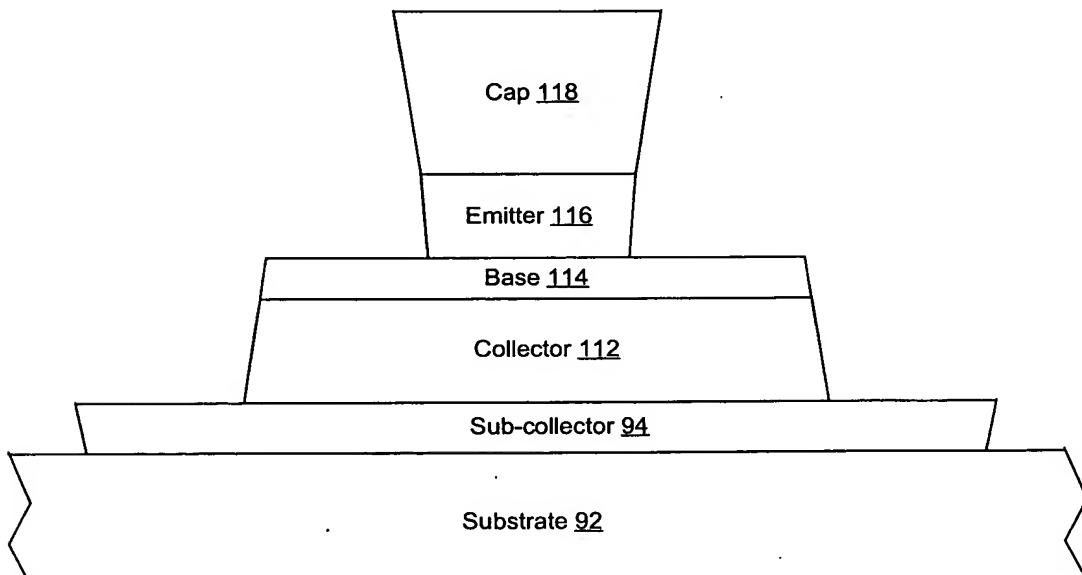


Fig. 6D

"SELF-ALIGNED PROCESS USING INDIUM GALLIUM ARSENIDE ETCHING TO FORM REENTRY FEATURE IN HETEROJUNCTION BIPOLAR TRANSISTOR"

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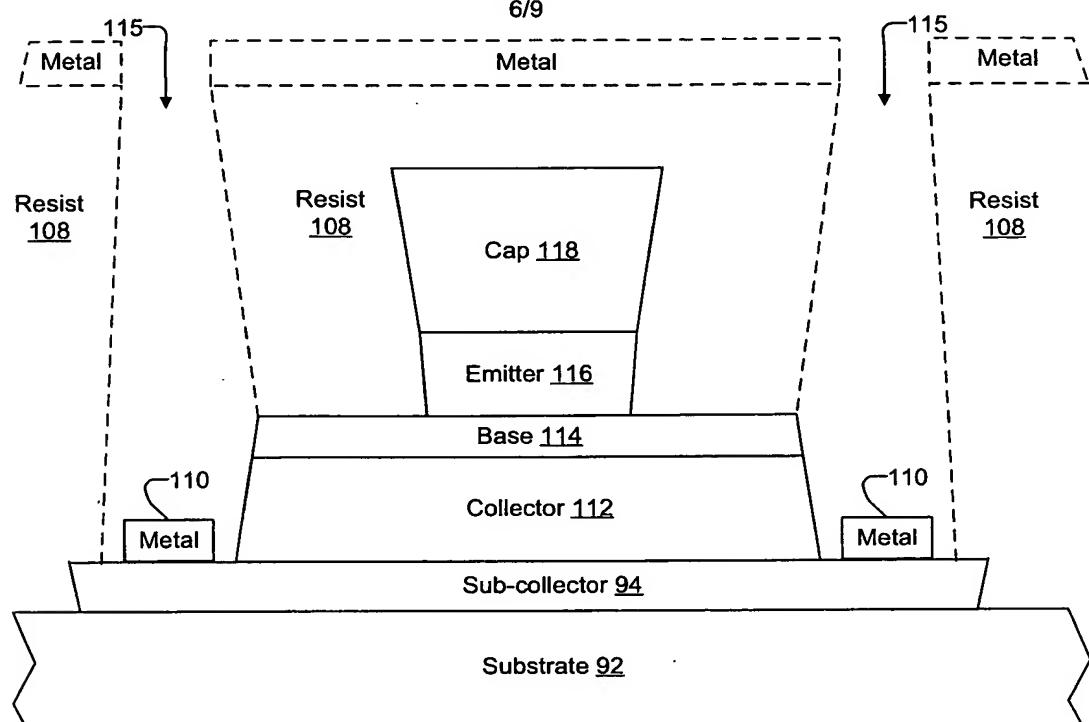


Fig. 6E

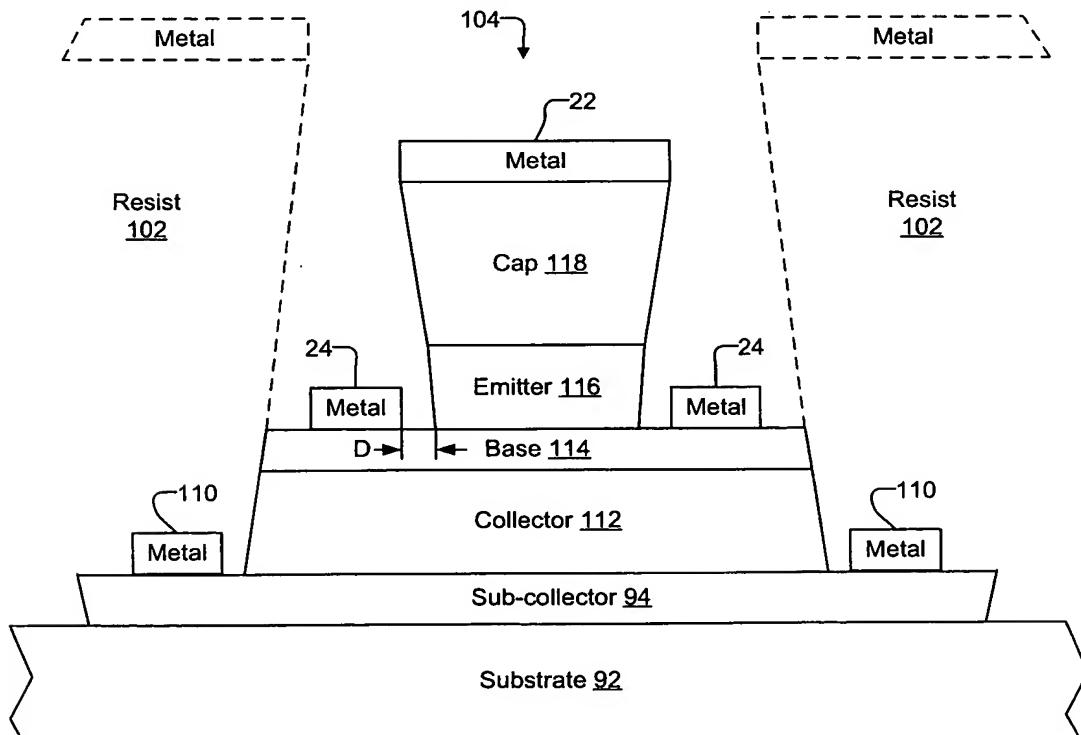


Fig. 6F

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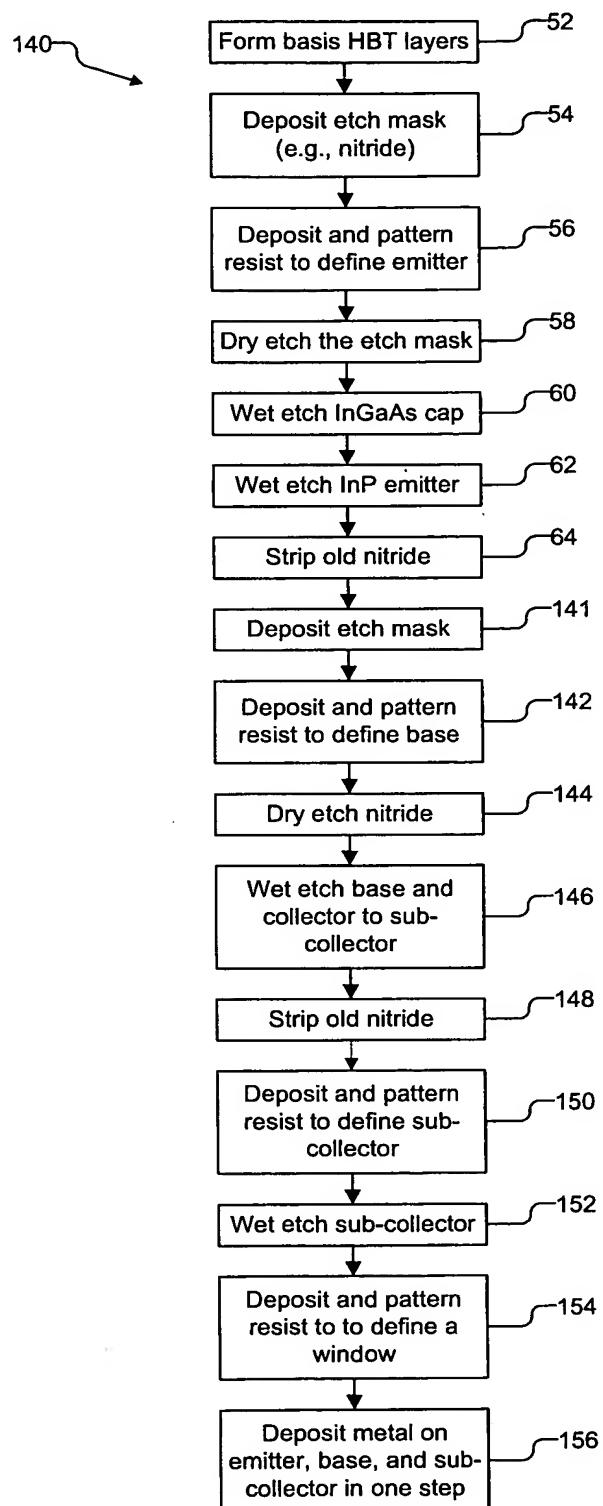


Fig. 7

"SELF-ALIGNED PROCESS USING INDIUM GALLIUM ARSENIDE ETCHING TO FORM REENTRY FEATURE IN HETEROJUNCTION BIPOLAR TRANSISTOR"

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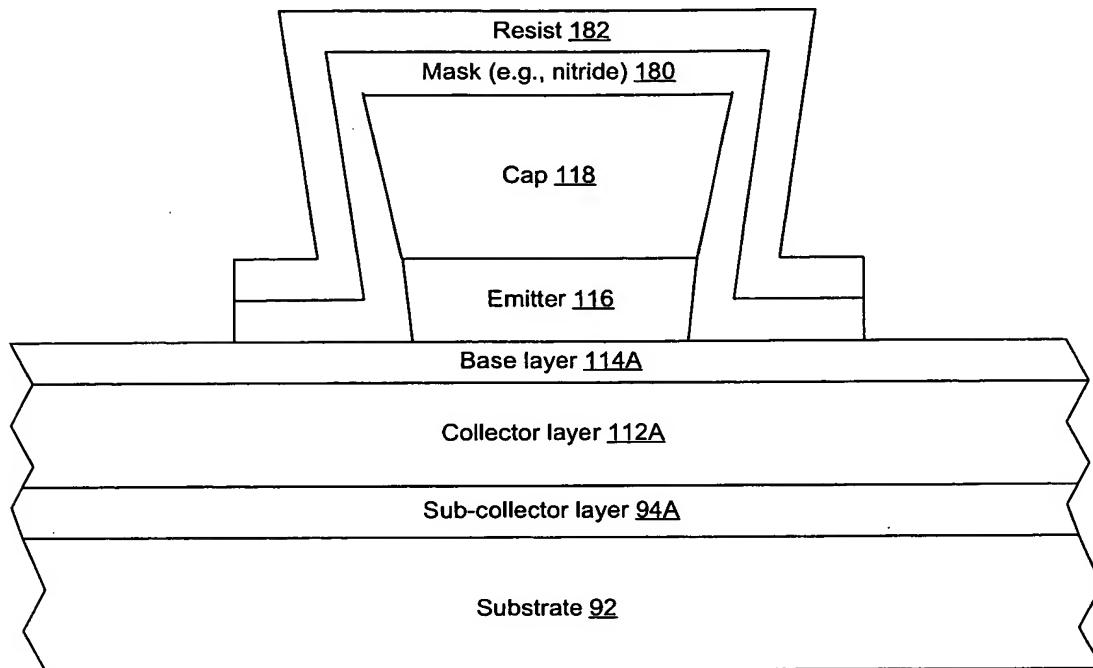


Fig. 8A

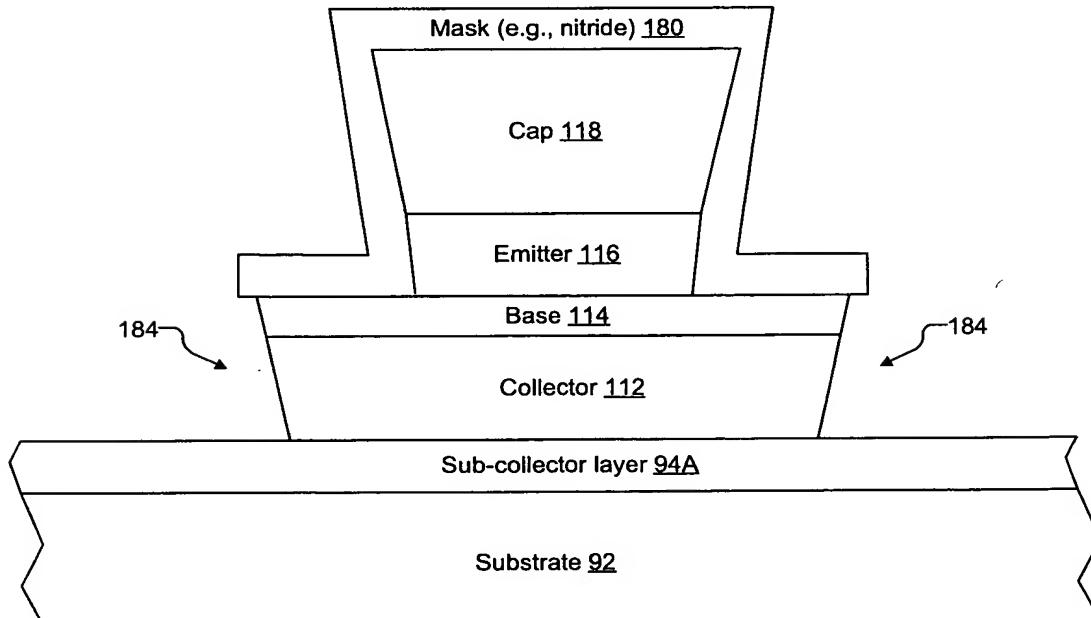


Fig. 8B

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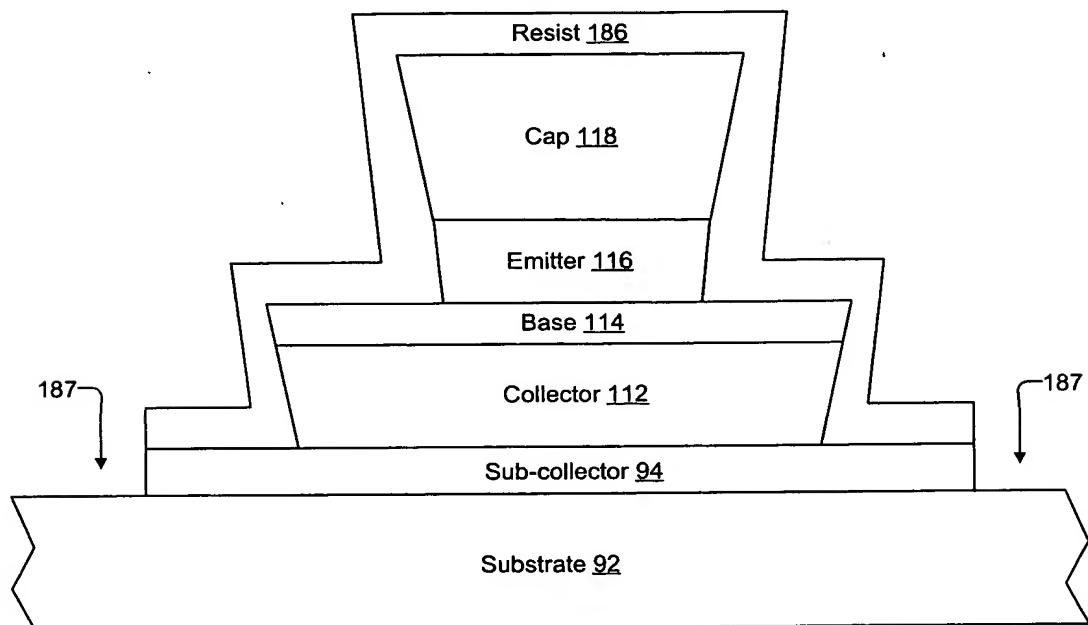


Fig. 8C

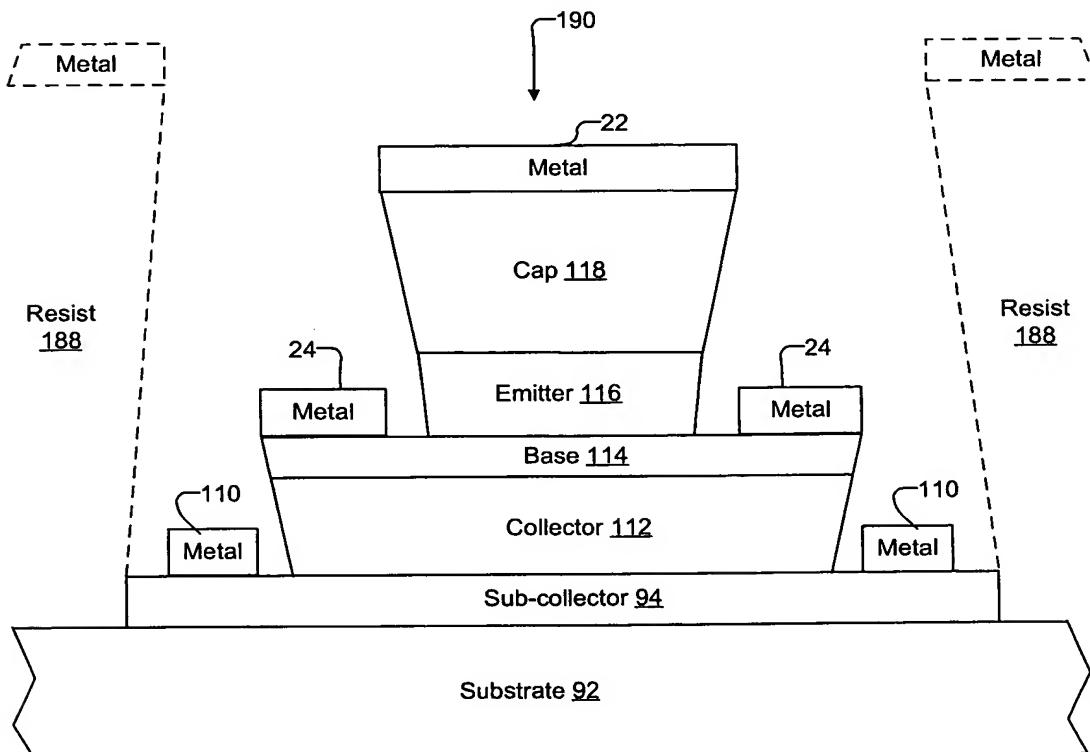


Fig. 8D